IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 51. (Cancelled)

52. (Original) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region and a peripheral circuit transistor forming region of a semiconductor substrate;

patterning said first conductive film lying over the memory cell forming region to form a first conductive pattern which serves as a first gate electrode of a memory cell and leaving said first conductive film over said peripheral circuit transistor forming region;

forming a second conductive film over said memory cell forming region and said first conductive film in said peripheral circuit transistor forming region; and

etching said second conductive film to form each second gate electrode of said memory cell on at least side walls of said first conductive pattern, and forming a gate electrode of each peripheral circuit transistor comprising said second conductive film and first conductive film over said peripheral circuit transistor forming region.

53. (Original) A method according to claim 52,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

54. (Original) A method according to claim 53,

wherein said peripheral circuit transistors include a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said first gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

55. (Original) A method according to claim 53, wherein said second gate electrode is formed on side walls of said first gate electrode through an insulating film in sidewall spacer fashion.

56. (Original) A method according to claim 53, wherein an electrode withdrawal portion of said second gate electrode is formed in said forming step of the second gate electrode.

57. (Original) A method according to claim 53, further including a step of patterning said first conductive pattern after said formation of the second gate electrode to thereby form said first gate electrode.

58. – 62. (Cancelled)

63. (Original) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region of a semiconductor substrate and forming an insulating film over said first conductive film;

etching said insulating film and said first conductive film to form a first conductive pattern which serves as a first gate electrode of a memory cell;

forming a second gate electrode of said memory cell on side walls of said first conductive pattern;

removing said insulating film over said first conductive pattern;

forming sidewall spacers, each comprised of an insulating film, in self-alignment with side walls of said second gate electrode; and

forming a silicide layer for each of said first conductive pattern and said second gate electrode in self-alignment with respect to said sidewall spacers.

64. (Original) A method according to claim 63,

wherein in said sidewall spacer forming step, said sidewall spacers are formed on said side walls on both sides of said second gate electrode and side walls of said first gate electrode,

wherein said silicide layer for said second gate electrode and said silicide layer for said first gate electrode are electrically isolated by said sidewall spacer disposed on one side of said both sides,

wherein said silicide layer for said second gate electrode and a silicide layer for a source region or a drain region are electrically isolated by said sidewall spacer on the other side thereof, and

wherein said silicide layer for said first gate electrode and said silicide layer for said source region or said drain region are electrically isolated by sidewall spacers formed on said side walls of said first gate electrode.

65. (Original) A method according to claim 63, wherein a gate electrode of each peripheral circuit transistor is formed of a film obtained by laminating a conductive film lying in the same layer as said first conductive film, and a second conductive film lying in the same layer as said memory gate electrode.

66. (Original) A method according to claim 63,

wherein sidewall spacers are formed on side walls of said gate electrode of the peripheral circuit transistor in said sidewall spacer forming step, and

wherein a silicide layer is formed over said gate electrode of said peripheral circuit transistor in said silicide layer forming step.

67. (Original) A method according to claim 63,

wherein said memory cell includes, in a memory cell forming region of a semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode disposed near one of said source and drain regions, a memory gate electrode disposed near the other of said source and drain regions, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

68. – 70. (Cancelled)

71. (Original) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region of a semiconductor substrate and forming an insulating film on said first conductive film;

etching said insulating film and said first conductive film to form a first conductive pattern which serves as a first gate electrode of a memory cell;

forming a second gate electrode of said memory cell on side walls of said first conductive pattern;

removing said insulating film over said first conductive pattern;

forming sidewall spacers, each comprised of an insulating film, in self-alignment with side walls of said second gate electrode; and

etching said first conductive pattern in self-alignment with respect to said sidewall spacers to form corresponding first gate electrode.

72. (Original) A method according to claim 71,

wherein a second gate insulating film is formed between said second gate electrode and said semiconductor substrate,

wherein said sidewall spacers are formed on said side walls on both sides of said second gate electrode,

wherein said second gate insulating film is formed in self-alignment with respect to said sidewall spacer on one side of said both sides, and

wherein said first gate electrode is formed in self-alignment with respect to said sidewall spacer on the other side thereof.

73. (Original) A method according to claim 71, wherein a gate electrode of each peripheral circuit transistor is formed of a film obtained by laminating a conductive film lying in the same layer as said first conductive film, and a second conductive film lying in the same layer as said memory gate electrode.

74. (Original) A method according to claim 71,

wherein said second gate insulating film includes a nonconductive charge trap film corresponding to a charge storage region,

wherein said first gate electrode constitutes a control gate electrode, and

wherein said second gate electrode constitutes a memory gate electrode and is formed on side walls of said control gate electrode through an insulating film in sidewall spacer fashion.

75. – 85. (Cancelled)